2020 17th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE)
Mexico City, Mexico. November 11-13, 2020

A Performance Comparative at Low Temperatures of Two FET Technologies: 65 nm and 14 nm

Omar López-L
Department of Electronics
INAOE
Puebla, México
omar.lopez@inaoep.mx

I. Martínez
Department of Electronics
INAOE
Puebla, México
ismael.mtzramos@ieee.org

D. Durini
Department of Electronics
INAOE
Puebla, México
ddurini@inaoep.mx

E.A. Gutiérrez-D
Department of Electronics
INAOE
Puebla, México
edmundo@inaoep.mx

D. Ferrusca
Department of Astrophysics
INAOE
Puebla, México
dferrus@gmail.com

M. Velázquez
Department of Astrophysics
INAOE
Puebla, México
miyang29@gmail.com

F.J. De la Hidalga
Department of Electronics
INAOE
Puebla, México
jhidalga@inaoep.mx

V. Gómez
Department of Astrophysics
INAOE
Puebla, México
vigoriv@gmail.com

***Abstract*—Since Moore's law has promoted a rapid evolution of FET technologies sometimes, key aspects stay unnoticed while novel nodes appear at the horizon. In this manuscript we present a study comparing the performance of the 65 nm MOSFET and the 14 nm SOI finFET technology, both at low temperatures, where main electrical parameters are analyzed. In the case of the MOSFET we cooled it down to 77 K, while for the finFET, we achieve to cooled it down to 340 mK. Thus, the intend of this work is to provide a vision of which technology is better at each application, such as quantum computing, astronomy, infrared and UV detectors, particle detectors, etc.**

***Index Terms*—Cryogenic electronics, Cryo-CMOS, Electrical Characterization, 65-nm, MOSFET, 14-nm, finFET, ZTC.**

I. Introduction

Every day new applications and requirements emerge for FET devices, and not always the ultimate available technological node represents de best solution for everything but there are some technologies capable to solve an specific requirement either cheaper or better performance even though both of them. Thus, the study and the comparative of ultimate technology with some previous one is crucial to optimize assets. In this manuscript a study of main parameters for two technologies was done, both at low temperatures. We could identify how each parameter was impacted by the thermal stress, providing us guidelines of how a specific technological node work at low temperatures.

II. Cryogenic Measurements

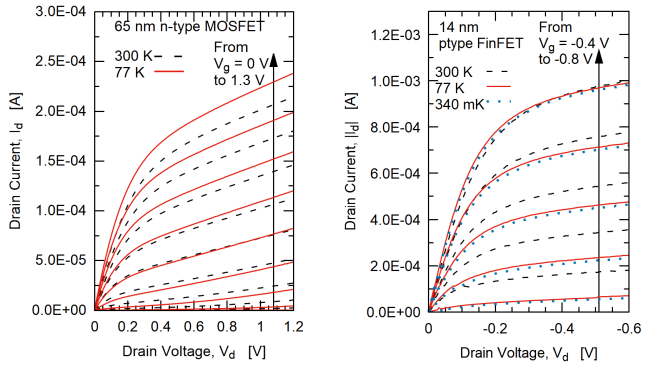
Regarding to the 65 nm MOSFET device, we used a planar n-type device, cooled into a LakeShore open cycle cryostat, This cryostat is able to work with Nitrogen and Helium and achieve 77 K and 4.2 K temperatures respectively, with a maximum power dissipation of 250mW at 4.2 K. The controller used was the DRC 93CA. The vacuum system is composed by a mechanical and a diffuser pump Combivac, achieving 10 mTorr. Previously the device was bonded onto a Ceramic Dual in Line Package for the manipulation. In this work, we achieved a temperature of 77 K, using liquid Nitrogen. On the other hand, regarding to the 14 nm SOI finFET, a p-type device was used, which was also placed onto C-DIP and bonded with Gold (Au) wires for electrical connection. The C-DIP was installed at the ultra-cooled-head stage with the aid of an aluminum sample holder. In this case, we used a close cycle Pulse Tube Cooler from Cold Edge to achieve 4 K temperatures, over the cold-plate it was installed a three-stage sub-Kelvin He^3He^4 cooler from Chase Research Cryogenics LTD with a power capacity of $\sim$ 3 μW at 340 mK, an Agilent B1500A Semiconductor Device Analyzer (SDA) was used to obtain electrical measurements and Manganin wire was used for electrical cabling on different stages from room temperature down to 340 mK due to its low thermal conductivity properties. All instruments located at the Astronomical Instrumentation Laboratory into the INAOE facilities.

III. Results

Output and transfer characteristics are shown in Fig. 1, 2 and 3, for 65 nm n-type MOSFET and 14 nm p-type finFET. Comparing output characteristics from Fig. 1, we can see the first important difference, the current handling, while for the 65 nm device we have an increase in the current by cooling it down to 77 K, the 14 nm device shows a decrease of current handling, this tendency is confirmed when we see the curve at T = 340 mK. Different scattering processes are involved in this behavior such as phonon and ionized impurities scattering, furthermore, two different type of carriers are involved, electron and holes for the 65 nm and 14 nm devices respectively; although the cooling process reduces phonon scattering, it is necessary more energy to activate carriers, even for the doping channels freeze-out phenomena can be seen [1].

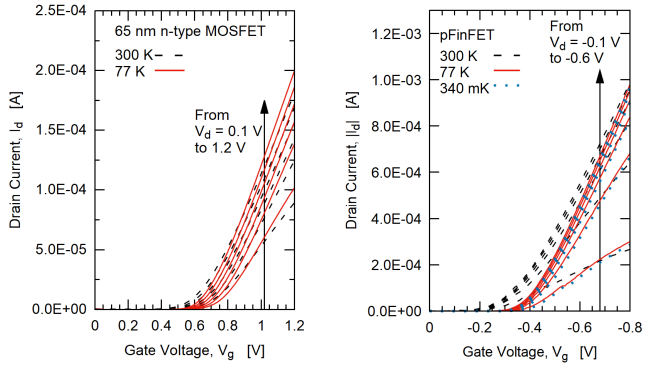
On the other hand, it is easy to see that the 65 nm device presents a smaller output resistance (R_{out}) than the 14 nm does, in this case, we have a resistance between 15kΩ and

978-1-7281-8987-1/20/$31.00 ©2020 IEEE



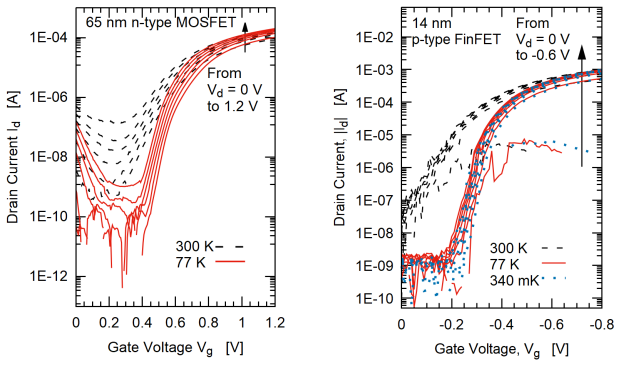
(a) (b)

Fig. 1: Output characteristics for both, a) 65 nm n-type MOSFET and b) 14 nm p-type finFET from 300 K down to 77 K, with step of 0.1 V



(a) (b)

Fig. 2: Transfer characteristics for both, a) 65 nm n-type MOSFET and b) 14 nm p-type finFET from 300 K down to 77 K, with step of 0.1 V



(a) (b)

Fig. 3: Transfer characteristics for both, a) 65 nm n-type MOSFET and b) 14 nm p-type finFET from 300 K down to 77 K, in semi-log format, with step of 0.1 V

13.6kΩ for the 65nm device for 300 K and 77 K respectively, meanwhile, for the 14 nm device we have 5MΩ and 2kΩ for 300 K and 77 K respectively, where the definition of output resistance is the following [2]:

$$R_{\text{out}} = \left(\frac{\partial I_{\text{d}}}{\partial V_{\text{d}}}\right)^{-1} | \textit{at saturation region.} \tag{1}$$

Additionally, comparing transfer characteristics we can see high leakage current for the 65 nm device at V_g = 0 V, which achieves its lowest level around 0.25 V and cooled at 77 K. In both cases a shift to higher threshold voltage (V_{th}) at low temperatures can be seen. Which is explained for the activation energy for carriers mentioned before. In addition, we can see that Subthreshold Slopes (SS) is decreasing in both cases, since we appreciate a sharper transition from turn-off to turn-on state. Having the following expression for SS:

$$SS = \frac{1}{Slope} = \frac{ln(10)nk_{\text{B}}T}{q} \approx \frac{60nT}{300} mV/dec \tag{2}$$

where k_{B} is the Boltzmann constant, T is the Temperature in Kelvin and n is is given by $n = 1 + (C_{\text{b}} + C_{\text{it}}/C_{\text{ox}})$, with C_b as the back capacitance, C_{it} as the interface trap capacitance and C_{ox} as the oxide capacitance [3].

One of the most important electrical parameters is the Threshold voltage (V_{th}), and comparing the increase percentage for each one we obtain the plot shown in Fig. 4, while for the 65 nm device we have an increment of 21% of V_{th} for the 14 nm device we have an increment of 143%, besides that in absolute values, we have a bigger threshold voltage for the 65 nm device than the other one, the reason is explained by the V_{th} definition [4]:

$$V_{\text{th}} = V_{\text{FB}} + \phi_0 + \gamma\left(\sqrt{\phi_0 + V_{\text{SB}}}\right) \tag{3}$$

where flat band voltage is defines as

$$V_{\text{FB}} = \phi_{\text{MS}} - \frac{Q_0{}'}{C_{\text{ox}}{}'} \tag{4}$$

with ϕ_{MS} as the sum of all contact potentials from gate, thourgh external connection, to bulk, $Q_0{}'$ is the effective interface charge per unit of area and $C_{\text{ox}}{}'$ is the total capacitance between the two ends of the oxide per unit of area. where surface potential (ψ_s) is pinned to a constant ϕ_0 defined as:

$$\phi_0 = 2\phi_{\text{F}} \tag{5}$$

with ϕ_{F} as the Fermi potential. The body effect coefficient (γ) and Source-Bulk Voltage V_{SB}. Therefore, we are going to have higher $C_{\text{ox}}{}'$ for the 14nm device, since t_{ox} is smaller, so V_{FB} increase its value, moreover, at smaller technological nodes, devices present higher doping profile along the channel, hence, ϕ_{F} increases its value, finally, ($\gamma \propto 1/C_{\text{ox}}{}'$), which also gives us a higher value, therefore, for all these contributions, it is expected to have a a higher V_{th} value for the 65 nm device than for the 14 nm device.

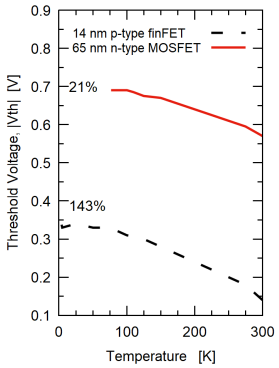


Fig. 4: Threshold Voltage V_{th} for both, 14 nm and 65 nm devices vs Temperature.

Nevertheless, the estimation of V_{th} is obtained indirectly and there are different methods for this, for instance, Ortiz-Conde et. al. [5], propose 11 different methods to extract V_{th}, in this case we use the constant-current method, which evaluates the V_{th} as the value of the gate voltage, V_g, corresponding to a given arbitrary constant drain current, I_d and $V_d < 100$ mV. In this case, V_{th} was obtained by setting a constant on-current, 1E-7 A for the 65 nm device and 1E-6 A for the 14 nm device. So, we can determine that the 65 nm device is more robust for its electrical parameter by cooling it.

In addition, in Fig. 5a we can see that both devices present a percentage increase in transconductance for V_d = abs(0.1) V condition, assuming the value of transconductance at 300 K as 100% and the actual value shown in Fig. 5b with an inset for illustrate the values for the 65 nm device. For the case of the 65 nm devices we can see that the highest point is located around 110 K. Transconductance is obtained by:

$$g_m = \frac{\partial I_d}{\partial V_g} | V_d = constant \tag{6}$$

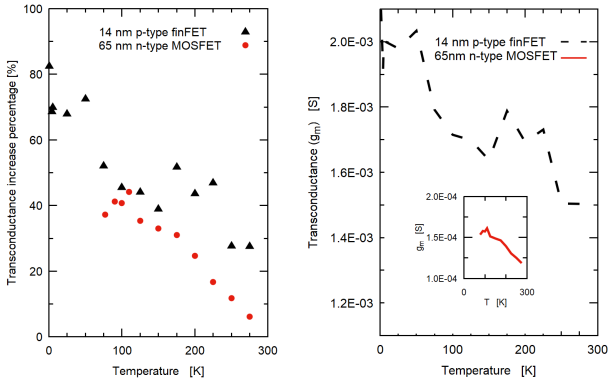


Fig. 5: Comparative of a) transconductance increase percentage and b) actual transconductance values for 65 nm and 14 nm devices.

Another important parameter is the majority carrier mobility, since we used a n-type MOSFET and a p-type finFET as a test vehicle, electrons and holes are majority carriers, respectively. In fact, for bulk-doped silicon and (100) orientation wafers, the mobility for electrons is more than two times bigger than for holes [3]. In Fig. 6a, we can see the relation between majority carrier mobility vs Temperature, having a comparison in a), where we can see a saturation below 100 K for case of 14 nm, while for the 65 nm device we see a peak value around 100 K and a decrease below that temperature.

In Fig. 6b we can see the behavior of hole mobility for the case of 14 nm device, from weak to strong inversion, and agrees with the theory explained by Peter Y. Yu [6], that at low temperatures and low electric field **E** applied to the channel we have higher values of mobility.

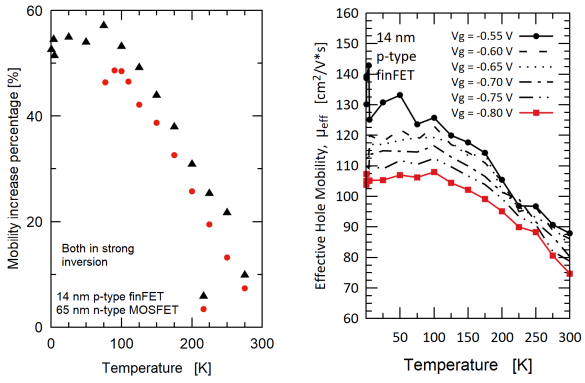


Fig. 6: a) Comparison of carrier mobility increase vs Temperature for the two devices, and b) hole mobility vs Temperature for the 14nm finFET.

The model used in order to extract the effective mobility is defined as follow [3]:

$$\mu_{\text{eff}} = \frac{g_d L}{W Q_n} \tag{7}$$

where transistor conductance, g_d, is given by:

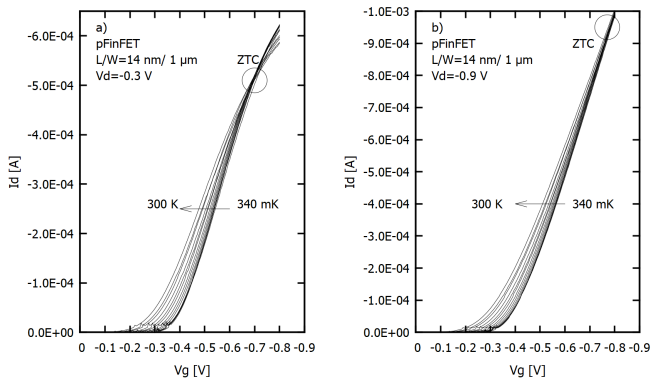
$$g_d = \frac{\partial I_d}{\partial V_d} |_{V_{gs} = \text{constant}}, \tag{8}$$

the mobile channel charge density, Q_n, can be calculates as follows:

$$Q_n = C_{ox}(V_g - V_{th}), \tag{9}$$

and W and L are the width and length of the transistor respectively [3].

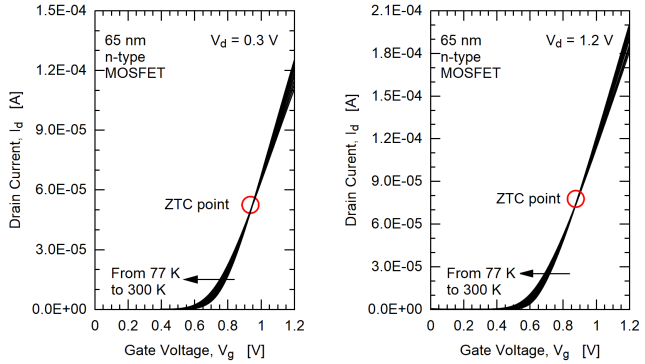
The Zero Temperature Coefficient (ZTC) is another important parameter related to the characterization at low temperatures, and it refers to a point where exists a mutual cancellation of the mobility and threshold voltage dependencies on temperature [7], In Fig. 7 we can see I_d-V_{gs} measurements, from 300 K down to 340 mK for a) V_{ds}= -0.3V and b) V_{ds}= –0.9 V. The ZTC shows a shift around -0.7V to -0.8V in V_{gs} as a function of drain voltage applied.



(a) (b)

Fig. 7: ZTC comparative from 300 K to 340 mK with a) Vd = -0.3V, b) Vd = -0.9V.

In Fig. 8 we can see that the ZTC point is located around 0.9 V. In general, since hole mobility is smaller than electron mobility, this point defines a larger gate bias voltage for the PMOS compared with the NMOS [7]. In this case we have two different technologies, so, what we can see is the fact that for the p-type finFET we found the ZTC point close to the maximum bias condition for V_g, that is, in strong inversion; unlike for the n-type MOSFET, where we find the ZTC point around the middle of the maximum bias for V_g, that is, weak-moderate inversion.



(a) (b)

Fig. 8: ZTC comparative from 300 K to 77 K with a) Vd = 0.3 V and b) Vd = 1.2 V.

IV. Conclusions

After the comparison of main electrical parameters, we can conclude that the 65 nm n-type MOSFET device is more robust at 77 K than the 14 nm p-type finFET device, first of all, because it presents only a 21% of **Threshold Voltage V_{th}** increase unlike the 143% increase for the 14 nm device, this behaviour is caused for the freeze out phenomena, reducing the inner energy of the devices, with a bigger influence for the 14 nm p-type finFET than for the 65 nm n-type MOSFET; secondly, in terms of **Transconductance and mobility**, the 65 nm device also presents slightly lower dependence to low temperatures, that is, there is less change percentage for the 65 nm device than for the 14 nm; and finally, the 65 nm device shows a **ZTC point** located around the weak-moderate inversion for both bias V_d = 0.3 V and 1.2 V, unlike the 14 nm device which shows its ZTC point at strong inversion, for both V_d conditions, this advantage is related to low power applications.

On the other hand, in absolute values, the 14 nm finFET presents higher drain current handling, as well as higher transconductance values (at V_d = 0.1 V), so here there exists a trade-off in order to choose which of these technologies could be more useful for a specific requirement, either you need more stability during the cooling process or you need to have more power handling. Finally we appreciated a reduction of 1% of the drain current for the 14 nm device from 300 K to 77 K, and a reduction of 1.7% down to 340 mK, meanwhile for the 65 nm device we could see an increment of 11.1% of drain current from 300 K to 77 K, both at strong inversion, phonon and impurity scattering is playing a key role in this situation.

Acknowledgment

We acknowledge CONACYT for supporting grants for Ph.D. studies with CVU. 737375 and CVU 626666.

References

[1] E.A. Gutierrez-D, M Jamal Deen y C.L. Claeys, “Low Temperature Electronics. Physics, Devices, Circuits and Applications,” Academic Press, 2001.
[2] B. Razavi, ”Fundamentals of Microelectronics”, 2nd. Edition, John Wiley & Sons, Inc., 2014.
[3] D. K. Schroder, “Semiconductor material and device characterization,” John Willy & Sons, inc., publication, 2006.
[4] Y. Tsividis, C. McAndrew, ”Operation and Modeling of the MOS Transistor,” 3rd ed., Oxford University Press, 2011.
[5] A- Otriz-Conde, et al., ”A revew of recent MOSFET threshold voltage extraction methods,” Microelectronics Reliability 42, 2002, pp 583-596.
[6] Peter Y. Yu, ”Fundamentals of Semiconductors, Physics and Materials Properties”, 4th edition, Springer, 2010.
[7] P. Toledo, H. K. (2014). ”Self-biased CMOS current reference based on the ZTC operation condition,” 2014, 27th Symposium on Integrated Circuits and Systems Design (SBCCI), 1-7.