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Reduced Capacitance Multiplier in Impedance-Mode with Large Scaling Factor and High Accuracy

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***Abstract*—A reduced capacitance multiplier based on an impedance-mode technique is presented. The architecture has large multiplication factor, high accuracy, and wide output swing. The multiplication factor and precision are based on passive devices that can be physically matched using proper layout techniques. To reduce energy consumption and area of silicon, a reduced number of devices was used compared to conventional circuits. Simulation results are included showing gains of 10, 100 and 1000. The topology of a floating equivalent capacitor is also presented. To test the functionality of the floating architecture simulation results of the circuit implemented in a biquadratic low-pass filter in 0.18 µm technology are presented.**

Keywords—Capacitor multiplier, Analog Integrated Circuits, low-voltage analog circuits

I. Introduction

Analog embedded systems generally require high-value high-accuracy linear capacitors that also occupy a small area of silicon. This is difficult to achieve since relatively small capacitors are obtained with modern manufacturing processes. Portability demands the implementation of smaller systems due to the great integration; this has motivated researchers and designers in recent years to develop a wide variety of architectures and methods to offer a large capacitive effect in a small area. In addition, in the design of capacitance multipliers two main parameters must be considered, the multiplication factor and the accuracy. Ingenious multiplication schemes have been presented that offer good precision but have a limited multiplication factor, reduced effective bandwidth, high power consumption and a large silicon area [1] - [3]. Other options have large multiplication factors and effective bandwidth; however, these are not accurate and have limited dynamic range [4] - [6]. Additionally, many of the featured circuits only offer the grounded implementation, which could be considered a disadvantage since the floating version is highly used in applications like biquadratic filters. This document introduces grounded and floating capacitance multipliers with large multiplication factor and high accuracy for reduced silicon area applications.

II. Capacitance Multiplication Techniques

A. Conventional Capacitance Multipliers

Conventional multiplier circuits are divided into two categories, current-mode and voltage-mode multipliers. The former is based on the amplified current copy, increasing the capacitive effect by means of a current mirror, where the size of one transistor is increased with respect to the other by a multiplication factor. Fig. 1 (a) shows a typical implementation, where the current is detected in a capacitor C, that is i_c, which is detected by transistor M1 connected in diode configuration and reflected in M2. If M2 is physically scaled k times with respect to M1, a current ki_c is induced in this transistor, resulting in an output current $i_o = i_c(1+k)$, from which an equivalent capacitance $C_{eq} = C\ (1\ +\ k)$, is obtained, where $1+k$, is the multiplication factor. These schemes offer high accuracy, with which good matching is achieved with proper layout techniques; however, the multiplication factor is generally a few tens, since the silicon area and the static power consumption are proportional to the multiplication factor. In addition, there is a decrease in effective bandwidth, given that the Equivalent Series Resistance (ESR) represents a moderately low resistance, of a few thousand ohms [1] - [3].

The second category, voltage-mode multipliers, are based on the Miller effect, where a capacitor C is connected to two nodes and can be conceptually reduced to equivalent capacitance values at each node with respect to ground. The value of capacitor C is multiplied by the voltage amplification of a gain stage, generally has the form $g_m r_o$, where g_m is the

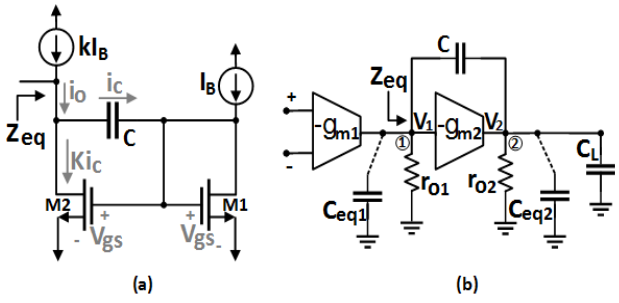

Fig. 1. Conventional capacitance multiplier: (a) current-mode and (b) voltage-mode.

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transconductance gain of a transistor and r_0 its output resistance. Fig. 1 (b) shows a two-stage differential amplifier, which is the typical implementation of this category. Miller's theory shows that the equivalent capacitance at node 1 is defined as $C_{\mathrm{eq1}} \approx g_{m2} r_{o2} C$, where g_{m2} is the transconductance gain and r_{o2} the output resistance of the second amplification stage; characteristic values range around a few hundreds. Furthermore, at node 2 the equivalent capacitance is defined as $C_{\mathrm{eq2}} \approx C$. Unfortunately, this type of multipliers has the drawback of a limited voltage amplitude at the output, since with large gain factors, the oscillation of the signal at key nodes can be distorted, introducing significant nonlinearities. In addition, they have low accuracy of the multiplication factor, as the term g_{m2} can have considerable variations due to the manufacturing process, the bias current and the temperature. The output resistance r_{o2} is highly dependent on the channel length modulation factor λ, which can vary significantly with the manufacturing process, temperature, and drain-source voltage. It is used only in applications where the multiplication factor is allowed to have large variations with a minimum required value [4], [5].

Lately, another type of multiplier has been studied, the impedance-mode multiplier. The concept of operation of this multiplier is based on establishing an output voltage according to the current detected at the same node, scaled by a multiplication factor. Fig. 2 shows the practical implementation [7]. The Flipped Voltage Follower (FVF) [8] is shown inside the broken lines, where the bias current I_{B} results in a constant voltage drop V_{GS2} in M2, operating as a voltage follower. Due to shunt feedback, transistor M1 has the ability to accept large currents, offering a very low output resistance, approximately $1/g_{\mathrm{m1}} g_{\mathrm{m2}} r_{\mathrm{o2}}$, as described in [8]. For the operation of the multiplier, M1 senses a current i_{d1} at the output node, which induces a voltage $v_{\mathrm{gs1}} = i_{\mathrm{d1}}/g_{\mathrm{m1}}$, that in the resistance R_{k} produces a current $i_{\mathrm{C}} = v_{\mathrm{gs1}}/R_{\mathrm{k}} = i_{\mathrm{d1}}/g_{\mathrm{m1}} R_{\mathrm{k}}$. This current i_{C} produces in the capacitor C a voltage v_{C} that is reflected at the output node by means of the FVF with a value $v_{\mathrm{C}} = i_{\mathrm{d1}}/sC g_{\mathrm{m1}} R_{\mathrm{k}}$; This defines an equivalent capacitance $C_{\mathrm{eq}} = C g_{\mathrm{m1}} R_{\mathrm{k}}$, where the multiplication factor is $k = g_{\mathrm{m1}} R_{\mathrm{k}}$. The FVF has reduced output swing, thus it is replaced by its Cascoded version (CFVF) [9], which is a follower modification that offers a wide output range equal to $V_{\mathrm{DD}} - V_{\mathrm{SS}} - 3V_{\mathrm{DSat}}$, and it also improves the output resistance to values of less than 1 Ω. Even though this multiplier allows large values of k and extended output oscillation, it has some drawbacks; for example, the need for a unit gain inverter, which increases energy consumption. It has low accuracy of the multiplication factor, since $g_{\mathrm{m1}} R_{\mathrm{k}}$, requires a good correspondence, as their values are defined by different types of devices; therefore, one is affected by different causes than the other. Furthermore, this structure does not allow the realization of the floating version, which could be very useful for applications such as biquadratic filters, where neither terminal of the capacitors are physically connected to ground.

B. Proposed Impedance-Mode Capacitor Multipliers

Before discussing a floating version, a grounded topology with one of the terminals of the capacitor connected to ground must be studied first, so it can later be implemented with the circuit's counterpart to offer the floating functionality.

The proposed multiplier takes advantage of the current sensing of current-mode multipliers and uses passive devices to produce a resulting output voltage. It is shown in Fig. 3, where the combination of resistors R_1 and R_2 form a voltage divider, particularly intended to modulate the induced current in the circuit and increase the capacitive effect. By using devices of the same type, the common-centroid layout technique may be employed, thus, parameter variations, due to fabrication process and temperature, affect both devices equally. This allows to have a design based on ratios rather that exact values, as provided by the voltage divider. Following this, an error of up to 0.1% matching accuracy between devices may be achieved according to [10], resulting in very high accuracy.

Assuming that a small signal current i_{o} is applied, a voltage $v_{\mathrm{gs1}} = i_{\mathrm{o}}/g_{\mathrm{m1}}$, is induced in M1, which is reflected at node x in the form $v_x = v_{\mathrm{gs1}} R_2/(R_1 + R_2)$. The current in M3 induces a voltage in capacitor C equal to $v_c = i_{\mathrm{d3}} Z_{\mathrm{C}}$, as $v_{\mathrm{sg3}} = v_x$, thus we have $v_c = v_x g_{\mathrm{m3}}/sC$. This voltage is used as the input to the FVF, setting the output voltage v_o to the value of v_c displaced by V_{GS2}. If a large multiplication factor is desired, R_1 must be large with respect to R_2 ; Assuming this, and an equal transconductance gain between M1 and M3, the above expression results in $v_c \approx (i_{\mathrm{d1}}/sC)(R_2/R_1)$, from which the equivalent capacitance is defined to be $C_{eq} = C(R_1/R_2)$, where R_1/R_2 is the multiplication factor k. Again, by matching devices R1 and R2 in the layout design high accuracy may be

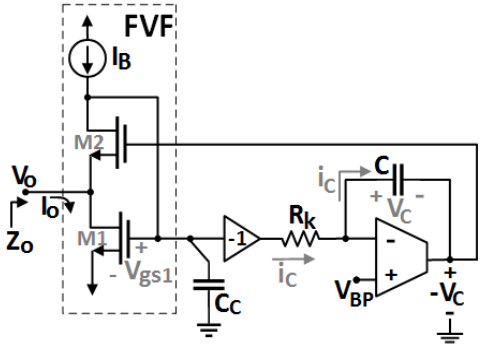

Fig. 2. Impedance-mode capacitance multiplier [7].

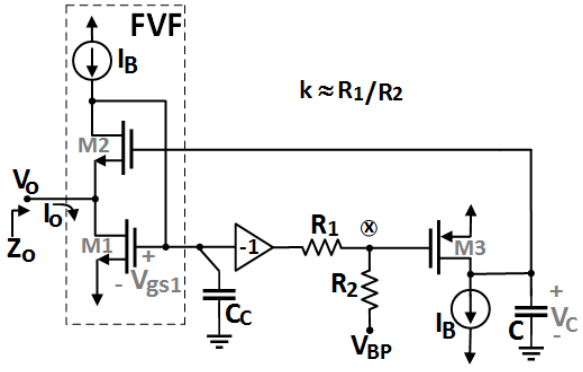

Fig. 3. Proposed impedance-mode capacitance multiplier, with high accuracy.

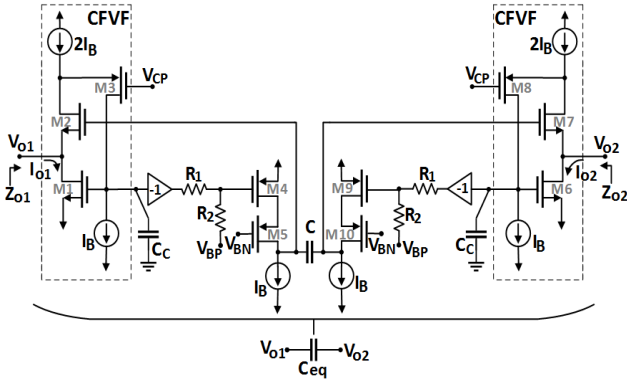

Fig. 4. Proposed floating capacitance multiplier.

achieved. In addition, in this implementation one of the terminals of capacitor C is physically connected to ground, allowing the implementation of the proposed floating version. This circuit is presented in Fig. 4, where two multipliers share a single capacitor. This structure already includes the CFVF for the extended output range. In DC operation, the multipliers are isolated; however, during dynamic operation, the capacitor is subject to the effect of both multipliers.

C. Frequency analysis

To define the effective bandwidth in which the implementation may be used as a capacitor, it is necessary to locate the frequency corners of the multiplier, then the circuit must be studied analytically. The grounded version of Fig. 3 with the conventional FVF is considered for simplicity. The FVF includes a shunt feedback, therefore, to ensure its frequency stability, a compensation capacitor C_C is included with a value of $C_C > 4C_L/(g_{m1}r_{o1})$ [8], where C_L is the load capacitance at the output node. The transfer function of the circuit is described from [7] as

$$Z_o = \frac{v_o}{i_o} = \left(\frac{1}{g_{m1}+sC_c}\right)\left[\frac{1+sC_c r_{o2}-g_{m2}r_{o2}H(s)}{1+g_{m2}r_{o2}}\right] \quad (1)$$

$$H(s) = \frac{R_2}{R_1+R_2}\left[\frac{-g_{m3}r_{o3}}{1+r_{o3}sC}\right] \quad (2)$$

Where $H(s)$ is the transfer function that comprises the devices R_1, R_2, M3 and capacitor C, where g_{m3} and r_{o3} are the transconductance gain and the output resistance of transistor M3, respectively. The overall transfer function of the multiplier is:

$$Z_o = \frac{(1+sC_c r_{o2})(R_1+R_2)(1+r_{o3}sC)+g_{m2}r_{o2}g_{m3}r_{o3}R_2}{(g_{m1}+sC_c)(R_1+R_2)(1+r_{o3}sC)(1+g_{m2}r_{o2})} \quad (3)$$

From where two poles and two complex conjugated zeros are defined:

$$\textit{poles} \quad \omega_{p1} = \frac{-1}{Cr_{o3}}; \qquad \omega_{p2} = \frac{-g_{m1}}{C_c}$$

$$\textit{zeros} \quad s^2[CC_c r_{o2}r_{o3}(R_1+R_2)] + s[C_c r_{o2}(R_1+R_2) + Cr_{o3}(R_1+R_2)] + R_1 + R_2 + g_{m2}r_{o2}g_{m3}r_{o3}R_2 = 0$$

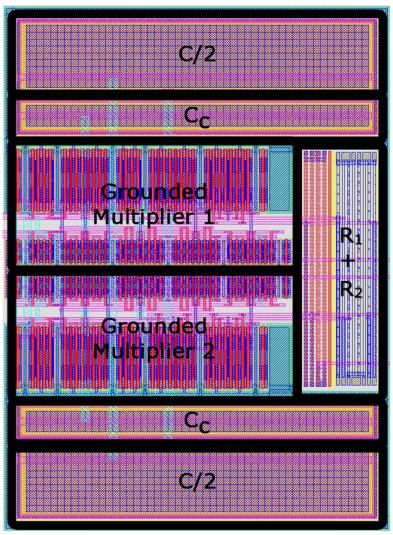

Fig. 5. Layout of the proposed multiplier circuit (82 µm x 60 µm).

III. Simulation Results

The proposed circuit was simulated in spectre in a 180 nm technology. Fig. 5 shows the layout of the circuit in Fig. 4. The nominal voltages are $V_{THN} = 0.4\,V$ and $V_{THP} = -0.6\,V$, and the sizes of the transistors are W/L = 9/0.36 and 27/0.36 µm/µm for NMOS and PMOS transistors, respectively. The circuit was tested with a supply voltage of $V_{DD} - V_{SS}$ = 3.2 V and a bias current of I_B = 50 µA. The values for the capacitors are C = 10 pF and C_C = 0.5 pF. With R_2 = 10 kΩ, values of R_1 = 100 kΩ, 1 MΩ and 10 MΩ were chosen to offer a multiplication factor of k = 10, 100 and 1000; the equivalent capacitance values are 150 pF, 1.5 nF and 15 nF, respectively. The deviation in C_{eq} is given by the transistors M2 and M7 which operate as voltage followers, and by the inverters, each of which contributes an extra gain of 0.25, therefore there is a factor of 0.5 in addition to k. Fig. 6 shows the simulated impedance of the circuit in Fig. 4.

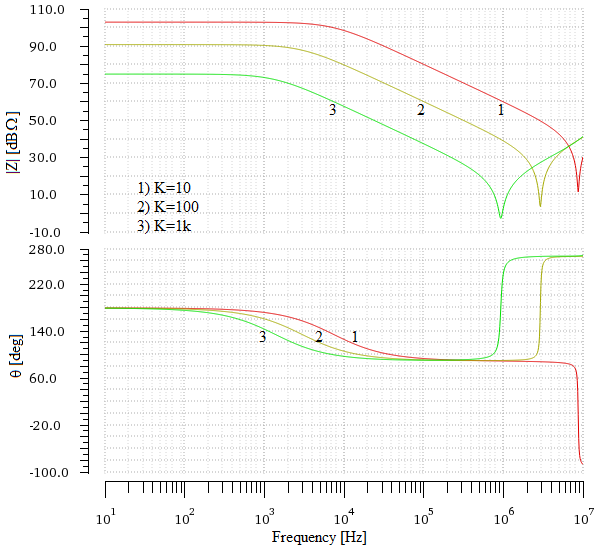

Fig. 6. Simulated impedance of the circuit in Fig. 4. split into magnitude and phase.

Biquadratic filter

To test the functionality of the proposed multiplier, it was implemented in a biquadratic low pass filter. The circuit of Fig. 7(a) [11] was considered for the filter, which has a transfer function of:

$$H(s) = \frac{\frac{R_Q R}{C_{eq}^2 R^3 R_Q}}{S^2 + \frac{C_{eq} R^3}{C_{eq}^2 R^3 R_Q} S + \frac{R_Q R}{C_{eq}^2 R^3 R_Q}} \quad (4)$$

From the previous transfer function is obtained: $Q = (C_{eq}^2 R^3 R_Q\ \omega_o)/(C_{eq} R^3)$, $\omega_o = \sqrt{(R_Q R)/(C_{eq}^2 R^3 R_Q)}$, from where the values for the quality factor Q and the cutoff frequency ω_o were derived. To offer a fully differential implementation of the filter, the structure of Fig. 7 (b) was also simulated using spectre in a 180 nm technology with the same supply voltages and bias current, $R = R_Q = 20k\Omega$ and equivalent capacitance values $C_{eq} = 0.15$, 1.5 and 15 nF. The results of the filter simulation are shown in Fig. 8.

Table I shows the results of the multiplier simulation. ω_{p1} defines the low frequency pole and ω_z the high frequency complex conjugate zeros; ω_{p2} is located at higher frequencies than the zeros, thus is not shown.

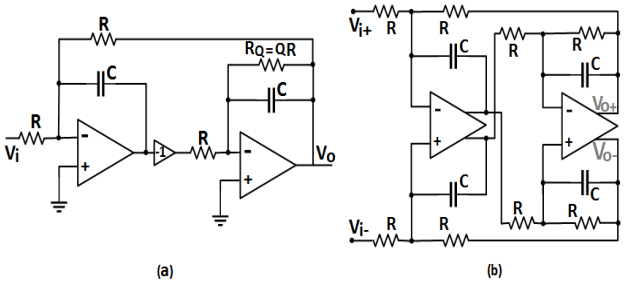

Fig. 7. Biquadratic filter to test the proposed circuit; (a) singled ended version, and (b) fully differential version.

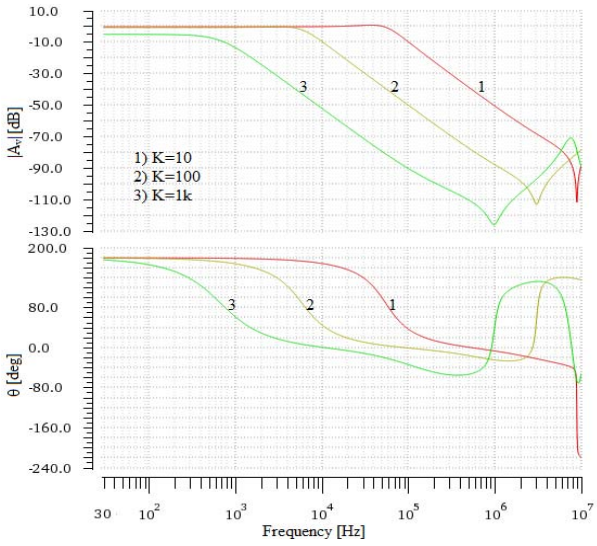

Fig. 8. Frequency response of the biquadratic filter of Fig. 7 (b), split into magnitude and phase.

TABLE I. RESULTS OF THE MULTIPLIER SIMULATION

Parameter	Multiplication Factor		
	10	***100***	***1000***
C_{eq} [nF]	0.15	1.5	15
Upper limit [kΩ](PLR)	140.5	35.2	5.7
Lower limit [Ω]	4.58	1.74	0.78
f_{p1} [kHz]	7.42	2.98	1.37
f_z [MHz]	8.63	2.88	0.93
f_o [kHz] (biquadratic filter)	67.8	6.7	0.678
Effective bandwidth [MHz]	8.62	2.87	0.92
Minimum supply voltage [V]	1.6	1.6	1.6
Static power consumption [mW]	1.28	1.28	1.28
THD [%] (biquadratic filter)	0.01298	0.0146	0.01295

IV. CONCLUSIONS

The realization of an impedance-mode capacitor multiplier based on current-voltage conversion with a high-performance voltage follower was presented. The circuit was shown to have a large scale factor and high accuracy, due to the use of passive devices that can be physically combined and the use of adequate layout techniques. Furthermore, it offers a larger output swing compared to voltage-mode topologies that are comparable in scale factor terms. The simulation results were presented, showing the operation of the floating architecture with a multiplication factor of up to 1000, implemented in a biquadratic low-pass filter to validate the proposed topology.

REFERENCES

[1] H. B. Le, X. D. Do, S. G. Lee, and S. T. Ryu, "A long reset-time power-on reset circuit with brown-out detection capability," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 58, no. 11, pp. 778–782, November 2011.

[2] I. C. Hwang, "Area-efficient and self-biased capacitor multiplier for onchip loop filter," Electron. Lett., vol. 42, no. 24, pp. 1392–1393, November 2006.

[3] S. Solis-Bustos, J. Silva-Martinez, F. Maloberti, and E. Sanchez-Sinencio, "A 60-dB dynamic-range CMOS sixth-order 2.4-Hz low-pass filter for medical applications," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 47, no. 12, pp. 1391–1398, December 2000.

[4] G. A. Rincon-Mora, "Active capacitor multiplier in Miller-compensated circuits," IEEE J. Solid-State Circuits, vol. 35, no. 1, pp. 26–32, January 2000.

[5] F. Bahmani and E. Sánchez-Sinencio, "A highly linear pseudo-differential transconductance," 30th IEEE European Solid-State Circuits Conference, Leuven, Belgium, pp. 111-114, September 2004.

[6] G. Palumbo, S. Pennisi, "Design methodology and advances in Nested-Miller compensation," IEEE Transactions on Circuits and Systems I, Fund. Theory and Applications, vol. 49, no. 7, pp. 893-903, July 2002.

[7] I. Padilla-Cantoya, "Capacitor multiplier with wide dynamic range and large multiplication factor for filter applications," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 60, no. 3, pp. 152-156, March 2013.

[8] R. Gonzalez *et al.*, "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 7, pp. 1276–1291, July 2005.

[9] J. Ramírez-Angulo *et al.*, "Comparison of conventional and new flipped voltage structures with increased input/output signal swing and current sourcing/sinking capabilities," in Proc. MWSCAS, Cincinnati, OH, USA, vol. 2, pp. 1151–1154, August 2005.

[10] T. C. Carusone, D. A. Johns, K. W. Martin, *Analog integrated Circuit Design*, 2nd ed. Hoboken, NJ: Wiley, 2012.

[11] H. Amir-Aslanzadeh, E. J. Pankratz, and E. Sánchez-Sinencio, "A 1-V +31 dBm IIP3, reconfigurable, continuously tunable, power-adjustable active-RC LPF," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 495–508, February 2009.